The Hot Path SSA Form
- Extension of Static Single Assignment (SSA) Form
- Only hot reaching definitions along frequent acyclic paths in program profiles reach respective uses
- Highly useful for Speculative Analyses and Optimizations
- Proposes an algorithm to construct Hot Path SSA
- Demonstrates effectiveness by designing analysis phase of a novel optimization (Speculative Sparse Conditional Constant Propagation, extension of Wegman and Zadeck's sparse conditional constant propagation)

Profiling k-Iteration Paths: A Generalization of Ball-Larus Profiling Algorithm:
- Ball-Larus Path Profiling - An Efficient technique to collect acyclic path frequencies of programs
- k-Iteration Paths - A Generalization of Ball-Larus Paths

Other Major Research Areas:
• Dynamic Voltage Frequency Scaling
• A new programming language for better exploitation of both inter-node and intra-node parallelism
• Transactional Memory performance optimization
• Power optimizations for VLIW architectures

Publications:
• TCP: Thread Contention Predictor, Aparna Mandke, Bharadwaj Amrutur, Y. N. Srikant and Chirnabji Bhattacharyya, To appear in PDP 2012
• Adaptive Power Optimization of On-Chip SNUCA Cache on Tiled Chip Multicores architectures using Remap Policy, Aparna Mandke, Bharadwaj Amrutur and Y. N. Srikant, SAC 2011
• Applying Genetic Algorithms to optimize power in tiled SNUCA Chip Multicore Architectures, Aparna Mandke, Bharadwaj Amrutur and Y. N. Srikant, SAC 2011
• Petrinet based Performance Modeling for effective DVS for multi-threaded programs, Arun R and Y. N. Srikant, SAC 2011
• Evaluation of Dynamic Voltage and Frequency Scaling for Stream Programs, Arun R and Y. N. Srikant, CF 2011
• Relative Roles of IC and CPI in WCET Estimation, Archana Ravindar and Y. N. Srikant, ICP 2011
• Probabilistic data-flow analysis using path profiles on structure graphs, Arun Ramamurthi and Y. N. Srikant, SIGSOFT FSE 2011

• Implications of Program Phase Behaviour on Timing Analysis, Archana Ravindar and Y. N. Srikant, INTERACT workshop associated with HPCA 2011
• Compiler assisted power optimizations for clustered VLIW architectures, Rahul Nagpal and Y. N. Srikant, Parallel Computing 2011
• Integrated energy aware cyclic and acyclic scheduling for clustered VLIW processors, Jimmy Bahuleyan, Rahul Nagpal and Y. N. Srikant, IPDPS workshops, 2010
• Accelerating Multi-Core Simulators, Aparna Mandke, Keshavan Varadarajan, Amrutur Bharadwaj and Y. N. Srikant, SAC 2010
• The Hot Path SSA Form: Extending the Static Single Assignment Form for Speculative Optimizations, Subhajit Roy and Y. N. Srikant, CC 2010
• Probabilistic Modeling of Data Cache Behaviour, Vinayak Puranik and Y. N. Srikant, EMSOFT 2009
• Profiling k-Iteration Paths: A Generalization of the Ball-Larus Profiling Algorithm, Subhajit Roy and Y. N. Srikant, CGO 2009

Adaptive Power Optimization in SNUCA Cache on Tiled Chip Multicores
- Leakage power consumption in caches contributes to major power dissipation in memory subsystem of the processor
- We propose a new method to estimate working set size of an application
- In case of over-allocation of cache, propose to switch off farther L2 cache banks and merge data from farther banks into nearer L2 banks
- This is done using remap policy on a tiled chip multicore platform
- Achieves improvements in execution time and energy savings

Adaptive Power Optimization in NUCA caches on Chip Multicores
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