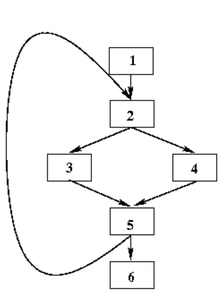
Department of Computer Science and Automation

The Hot Path SSA Form: Extending the Static Single Assignment Form for Speculative Optimizations:

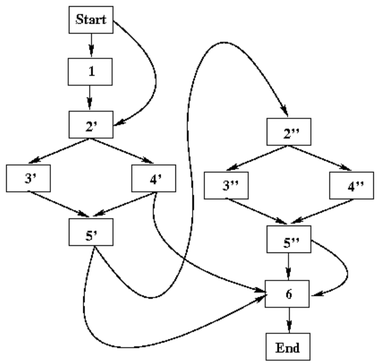
- Extension of Static Single Assignment (SSA) Form
- Highly useful for Speculative Analyses and Optimizations
- Only hot reaching definitions along Frequent Acyclic Paths in Program Profile reach respective uses

Profiling k-Iteration Paths: A Generalization of Ball-Larus Profiling Algorithm:

- Ball-Larus Path Profiling – An Efficient technique to collect acyclic path frequencies of programs
- k-Iteration Paths: A Generalization of Ball-Larus Paths spanning up to k iterations of a loop



A Simple Loop



Two Iteration Loop Unrolled DAG for 2–Iteration Path Profiling

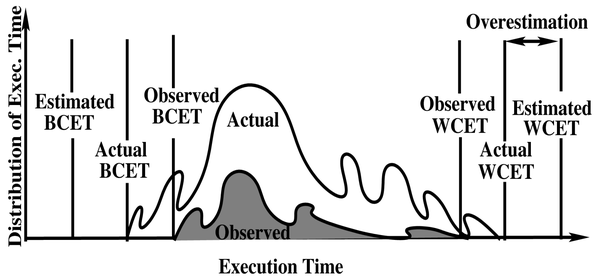
Profiling k-Iteration Paths: A Generalization of Ball-Larus Profiling Algorithm

Dynamic Voltage and Frequency Scaling:

- Energy and Power: Limit Performance, Affect System Reliability, A Concern for Environment
- Dynamic Power: Proportional to the Square of Operating Voltage and Frequency
- Static Power: At-least linear in Operating Voltage
- Dynamic Voltage and Frequency Scaling – Alter Operating Voltage and Frequency at Run Time
- Meet Performance Constraints

Special Focus:

- Software Based Frequency and Voltage Scaling for
  - Sequential Programs running on Multiple Clock Domain Processors
  - Concurrent Programs running on CMPs
- Uses Petri net based Program Performance Models for estimating performance of program regions with different voltage and frequency setings
- Chooses the least setting that meets performance constraints



Worst Case Execution Time Analysis

Image-Courtesy: The Compiler Design Handbook – Optimizations and Machine Code Generation;
Second Edition; CRC Press; Edited by Y.N.Srikant and Priti Shankar

Worst Case Execution Time Analysis (WCET):

- Critical for building Real Time Systems.
- Static WCET: Estimating WCET of a program before it is run.
- Dynamic WCET: Estimating Worst Case Completion Time of a program once it starts running.

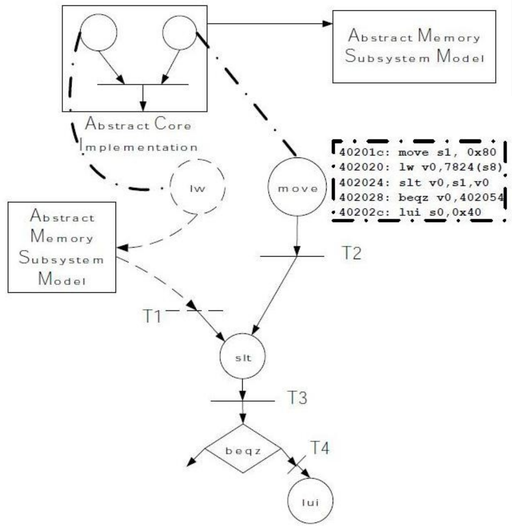
Special Focus:

1. Hybrid WCET Analyzer:
   - Factors WCET into Worst Case Instruction Count (WC IC) and Worst Case Clocks Per Instruction (WC CPI)
   - Estimates WC IC Statically, and WC CPI by Measurement
   - Exploits Program Phase Behaviour in reducing Instrumentation Overhead without reducing accuracy
   - Insight into Program IC and CPI relation helps in
     - Benchmark Classification in context of WCET Analysis
     - Optimizing beyond WC IC and WC CPI
2. Probabilistic Modeling of Multi-Level Data Cache:
   - Uses Static Program Analysis
   - Data Cache modeled using probabilistic access history
   - Data Cache Model Used to estimate Average Memory Access Time of data accesses

Simple Abstractions for Concurrent Programming:

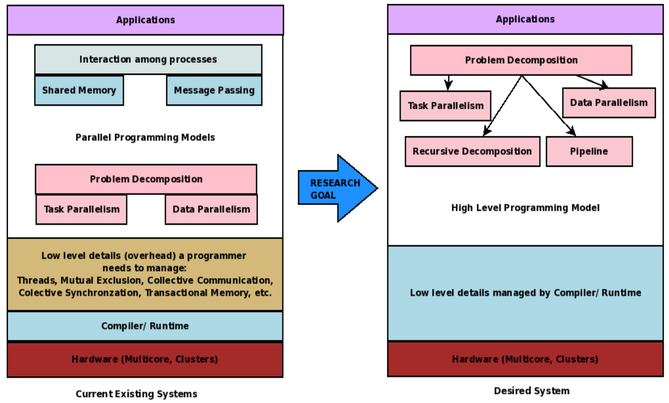
Goals:

- Identification of Interactions between Programming Models, Application Domains and Hardware
- Designing Simple, High Level Abstractions for Concurrent Programming
- Optimizing Application Performance, leveraging information from abstractions



Accelerating Multi-Core Simulators

Simple Abstractions for Concurrent Programming



Accelerating Multi-Core Simulators

- Simulators – Critical Tool in assessing benefits of micro-architectural designs and choices
- Useful for Design Space Exploration also
- Major drawback: Orders of magnitude slower than real machines
- Worse for Multi-Core Simulators
- Major Trade-off: Speed (Functional) and Accuracy (Detailed) of Simulators
- Special Focus:
  - Abstraction of Core Implementation
  - Use of these abstract models for estimation of execution time

Other Major Research Areas:

- A New Programming Language for better exploitation of both inter-node and intra-node parallelism
- Performance Improvement of Hybrid Transactional Memory Systems

Some Recent Publications:

- Evaluation of Dynamic Voltage and Frequency Scaling for Stream Programs (Arun R, Y. N. Srikant; To Appear: CF 2011)
- Relative Roles of IC and CPI in WCET Estimation (Archana, Y.N. Srikant; To Appear: ICPE 2011)
- Implications of Program Phase Behaviour on Timing Analysis (Archana, Y.N. Srikant; INTERACT 2011)
- Compiler Assisted Power Optimization for Clustered VLIW Architectures (Rahul Nagpal, Y. N. Srikant; Parallel Computing Jan 2011)
- The Hot Path SSA Form: Extending the Static Single Assignment Form for Speculative Optimizations (Subhajit Roy, Y.N. Srikant; CC 2010)
- Accelerating Multi-Core Simulators (Aparna Mandke, Keshavan Varadarajan, Amrutur Bharadwaj, Y.N. Srikant; SAC 2010)
- Probabilistic Modeling of Data Cache Behaviour (Vinayak Puranik, Y.N. Srikant; EMSOFT 2009)
- Profiling k-Iteration Paths: A Generalization of the Ball-Larus Profiling Algorithm (Subhajit Roy, Y.N. Srikant; CGO 2009)
- Compiler Directed Frequency and Voltage Scaling for a Multiple Clock Domain Microarchitecture (Arun R, Rahul Nagpal, Y.N. Srikant; CF 2008)
- Pragmatic Integrated Scheduling for Clustered VLIW Architectures (Rahul Nagpal, Y. N. Srikant; Software – Practice and Experience 2008)
- INTACTE: An Interconnect Area, Delay and Energy Estimation Tool for Microarchitectural Explorations (Rahul Nagpal, Arvind Madan, Bharadwaj Amrutur, Y.N. Srikant; CASES 2007)
- WCET Estimation for Executables in Presence of Data Caches (Rathijit Sen, Y.N. Srikant; EMSOFT 2007)

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