Compiler Lab

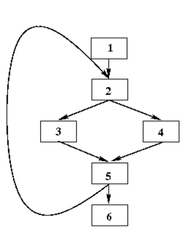
Department of Computer Science and Automation

The Hot Path SSA Form

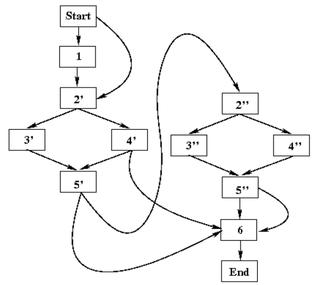
- Extension of Static Single Assignment (SSA) Form
- Only hot reaching definitions along frequent acyclic paths in program profile reach respective uses
- Highly useful for Speculative Analyses and Optimizations
- Proposes an algorithm to construct Hot Path SSA
- Demonstrate effectiveness by designing analysis phase of a novel optimization (***Speculative Sparse Conditional Constant Propagation***, extension of Wegman and Zadeck's sparse conditional constant progogation)

Profiling k-Iteration Paths: A Generalization of Ball-Larus Profiling Algorithm:

- Ball-Larus Path Profiling – An Efficient technique to collect acyclic path frequencies of programs
- k-Iteration Paths: A Generalization of Ball-Larus Paths



A Simple Loop



Two Iteration Loop Unrolled DAG for 2–Iteration Path Profiling

Other Major Research Areas:

- Dynamic Voltage Frequency Scaling
- A new programming language for better exploitation of both inter-node and intra-node parallelism
- Transactional Memory performance optimization
- Power optimizations for VLIW architectures

Worst Case Execution Time (WCET) Analysis

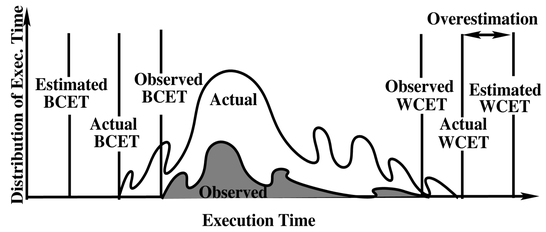


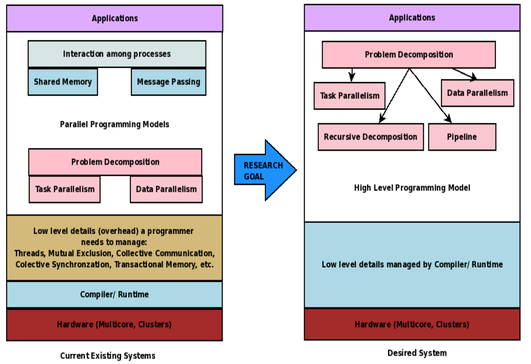
Image-Courtesy: The Compiler Design Handbook – Optimizations and Machine Code Generation; Second Edition; CRC Press; Edited by Y.N.Srikant and Priti Shankar

- Knowledge of WCET
  - Critical in Real Time System Design
  - WCET also helps in effective resource scheduling.

Special Focus:

1. Formulation of WCET:
   - Considers execution time as product of Instruction Count (IC) and Cycles Per Instruction (CPI)
   - WCET = Max(IC) X Max(CPI)
   - Estimates Max(IC) Statically, and Max(CPI) by measurement
   - Viewing execution time in terms of CPI helps exploits ***Program Phase Behaviour*** in reducing instrumentation overhead without reducing accuracy
   - Insight into Program IC and CPI relation helps in
     - Benchmark Classification in context of WCET Analysis
     - Optimizing beyond Max(IC) X Max(CPI)
2. Cache analysis for Multi-Level Data Caches:
   - Uses Static Program Analysis
   - Non-trivial for Multi-level data caches due to writebacks
   - Proposes an abstract lattice to make analysis more precise
   - Also improves original *may-analysis* for single level caches
   - Detects and rectifies serious flaw in original persistence analysis for single level caches

Simple Abstractions for Concurrent Programming:



Goals:

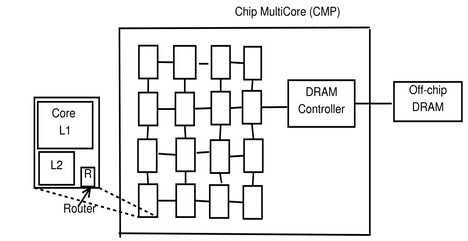
1. Identification of Interactions between Programming Models, Application Domains and Hardware

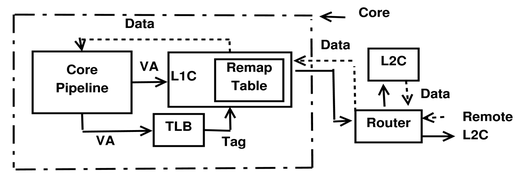
2. Designing Simple, High Level Abstractions for Concurrent Programming for Streaming Applications

3. Optimizing Application Performance, leveraging information from abstractions designed/adopted

4. Design a high-level Parallel Programming Model to reduce programmer overhead i.e. discover parallelism, communication management, for a complete streaming/multimedia application.

Adaptive Power Optimization in SNUCA Cache on Tiled Chip Multicores using Remap Policy





L1C - L1 Cache Controller, L2C - L2 Cache Controller
TLB - Translation Lookaside Buffer, VA - Virtual Address

Adaptive Power Optimization in NUCA caches on Chip Multicores

- Leakage power consumption in caches contributes to major power dissipation in memory subsystem of the processor
- We propose a new method to estimate working set size of an application
- In case of over-allocation of cache, propose to switch off farther L2 cache banks and merge data from farther banks into nearer L2 banks
- This is done using remap policy on a tiled chip multicore platform
- Achieves improvement in execution time and energy savings

Publications:

- ***TCP: Thread Contention Predictor,*** Aparna Mandke, Bharadwaj Amrutur, Y. N. Srikant and Chiranjib Bhattacharyya, To appear in ***PDP – 2012***
- ***Adaptive Power Optimization of On-Chip SNUCA Cache on Tiled Chip Multicore Architectures using Remap Policy***, Aparna Mandke, Bharadwaj Amrutur and Y. N. Srikant, ***IEEE workshop associated with SBAC-PAD 2011***
- ***Applying Genetic Algorithms to optimize power in tiled SNUCA Chip Multicore Architectures***, Aparna Mandke, Bharadwaj Amrutur and Y. N. Srikant, ***SAC 2011***
- ***Petrinet based Performance Modeling for effective DVS for multi-threaded programs,*** Arun R and Y. N. Srikant, ***SAC 2011***
- ***Evaluation of Dynamic Voltage and Frequency Scaling for Stream Programs,*** Arun R and Y. N. Srikant, ***CF 2011***
- ***Relative Roles of IC and CPI in WCET Estimation,*** Archana Ravindar and Y.N. Srikant, ***ICPE 2011***
- ***Probabilistic data-flow analysis using path profiles on structure graphs,*** Arun Ramamurthi and Y. N. Srikant, ***SIGSOFT FSE 2011***
- ***Implications of Program Phase Behaviour on Timing Analysis,*** Archana Ravindar and Y.N. Srikant***, INTERACT workshop associated with HPCA 2011***
- ***Compiler assisted power optimizations for clustered VLIW architectures,*** Rahul Nagpal and Y. N. Srikant, ***Parallel Computing 2011***
- ***Integrated energy aware cyclic and acyclic scheduling for clustered VLIW processors,*** Jimmy Bahuleyan, Rahul Nagpal and Y. N. Srikant, ***IPDPS workshops, 2010***
- ***Accelerating Multi-Core Simulators,*** Aparna Mandke, Keshavan Varadarajan, Amrutur Bharadwaj and Y.N. Srikant, ***SAC 2010***
- ***The Hot Path SSA Form: Extending the Static Single Assignment Form for Speculative Optimizations,*** Subhajit Roy and Y.N. Srikant, ***CC 2010***
- ***Probabilistic Modeling of Data Cache Behaviour,*** Vinayak Puranik and Y.N. Srikant, ***EMSOFT 2009***
- ***Profiling k-Iteration Paths: A Generalization of the Ball-Larus Profiling Algorithm,*** Subhajit Roy and Y.N. Srikant***, CGO 2009)***

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